**HIGH-PRECISION SMALL-PACKAGE VOLTAGE DETECTOR**

# S-808xxC Series

The S-808xxC series is a series of high-precision voltage detectors developed using CMOS process. The detection voltage is fixed internally with an accuracy of ±2.0%. Two output forms, Nch open-drain and CMOS output, are available. Ultra-low current consumption and miniature package lineup can meet demand from the portable device applications.

## ■ Features

- Ultra-low current consumption
  0.8 μA typ. (at $V_{DD}$=3.5 V)
- High-precision detection voltage
  ±2.0%
- Hysteresis width
  5 % typ.
- Operating voltage range
  0.95V to 10.0 V
- Detection voltage
  1.5 V to 6.0 V (0.1V step)
- Output form
  Active low Nch open-drain output or active low CMOS output

## ■ Applications

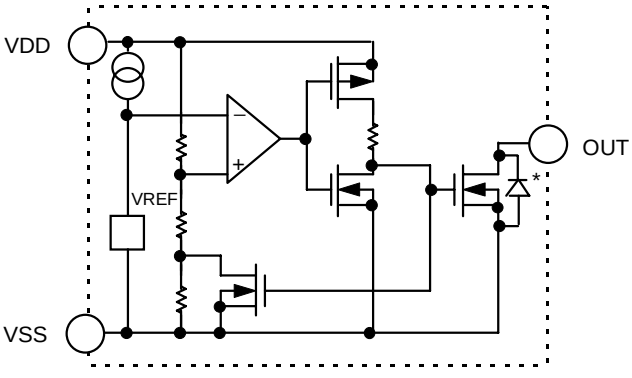
- Power monitor for portable equipment such as note book computers, digital cameras, PDA, and cellular phones.
- Constant voltage power monitor for cameras, video equipment and communication devices.
- Power monitor for microcomputers and reset for CPUs.
- Battery checker
- Detection of power failure

## ■ Packages

| | |
|---|---|
| 3-pin SOT-89-3 | (Package drawing code: UP003-A) |
| 3-pin TO-92 | (Package drawing code: YF003-A) |
| 4-pin SC-82AB | (Package drawing code: NP004-A) |
| 4-pin SNB(B) | (Package drawing code: BB004-A) |
| 5-pin SOT-23-5 | (Package drawing code: MP005-A) |

## ■ Block Diagrams

(1) Active low Nch open-drain output




(2) Active low CMOS output

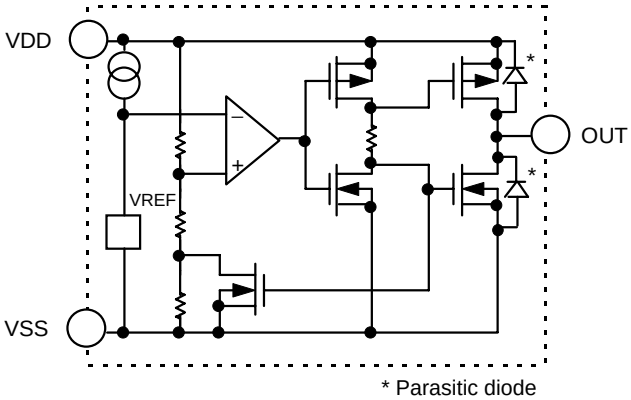



**Figure 1 Block Diagram**

## ■ Pin Configuration

See the attached drawings for details of the package.

SC-82AB
Top view

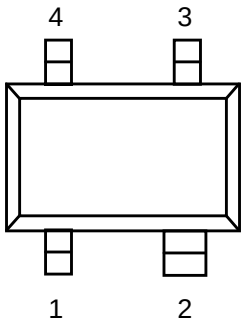


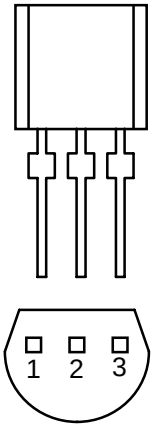

**Figure 2 Pin Configuration**

**Table 1 Pin Description**

| No. | Symbol | Description |
|---|---|---|
| 1 | OUT | Voltage detection output pin |
| 2 | VDD | Voltage input pin |
| 3 | N.C. (1) | non-connected |
| 4 | VSS | Ground pin |

(1) N.C. pin is electrically open.
Connecting this pin to VDD or VSS is allowed.

TO-92
Top view




Bottom view

**Figure 3 Pin Configuration**

**Table 2 Pin Description**

| No. | Symbol | Description |
|---|---|---|
| 1 | OUT | Voltage detection output pin |
| 2 | VDD | Voltage input pin |
| 3 | VSS | Ground pin |

SOT-89-3
Top view

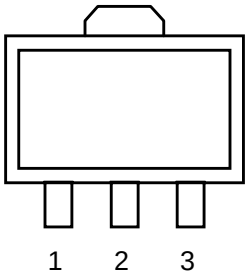



**Figure 4 Pin Configuration**

**Table 3 Pin Description**

| No. | Symbol | Description |
|---|---|---|
| 1 | OUT | Voltage detection output pin |
| 2 | VDD | Voltage input pin |
| 3 | VSS | Ground pin |

SOT-23-5
Top view

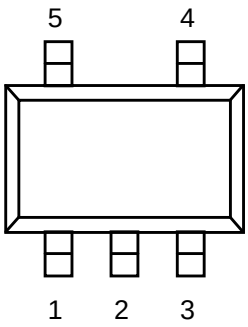



**Figure 5 Pin Configuration**

**Table 4 Pin Description**

| No. | Symbol | Description |
|---|---|---|
| 1 | OUT | Voltage detection output pin |
| 2 | VDD | Voltage input pin |
| 3 | VSS | Ground pin |
| 4 | N.C. (1) | non-connected |
| 5 | N.C. (1) | non-connected |

(1) N.C. pin is electrically open.
Connecting this pin to VDD or VSS is allowed.

4-pin SNB(B)
Top view

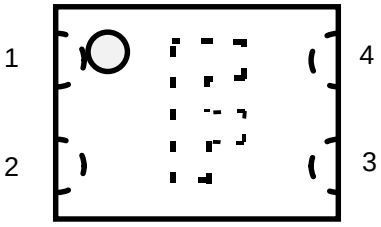



**Figure 6 Pin Configuration**

**Table 5 Pin Description**

| No. | Symbol | Description |
|---|---|---|
| 1 | OUT | Voltage detection output pin |
| 2 | VSS | Ground pin |
| 3 | N.C. (1) | non-connected |
| 4 | VDD | Voltage input pin |

(1) N.C. pin is electrically open.
Connecting this pin to VDD or VSS is allowed.

## ■ Selection Guide

S-808xx C x xx - xxx - xx

- Directions of the IC in tape form.(2)
  - TF:SNB(B)
  - T2:SOT-23-5
  - None:TO-92
- Product code (1)
- Package code
  - BB:SNB(B)
  - NB:SC-82AB
  - MC:SOT-23-5
  - UA:SOT-89-3
  - Y :TO-92
- Output form
  - N:Nch open-drain (active low output)
  - L:CMOS (active low output)
- Detection voltage (Detection voltage x 10)

(1):Please refer table 6 and 7 for product code.
(2) Please refer taping drawings at the end this book for directions of this IC in tape form.

**Table 6 Selection Guide**

(1/2)

| Detection voltage range | Hysterisis (typ.) | Nch Open-drain (Active low) | | | | |
|---|---|---|---|---|---|---|
| | | SC-82AB | TO-92* | SOT-89-3 | SOT-23-5 | SNB(B) |
| 1.5 V± 2.0% | 0.075V | S-80815CNNB-B8A-T2 | S-80815CNY-X | S-80815CNUA-B8A-T2 | — | — |
| 1.6 V± 2.0% | 0.080V | S-80816CNNB-B8B-T2 | S-80816CNY-X | S-80816CNUA-B8B-T2 | — | — |
| 1.7 V± 2.0% | 0.085V | S-80817CNNB-B8C-T2 | S-80817CNY-X | S-80817CNUA-B8C-T2 | S-80817CNMC-B8C-T2 | — |
| 1.8 V± 2.0% | 0.090V | S-80818CNNB-B8D-T2 | S-80818CNY-X | S-80818CNUA-B8D-T2 | S-80818CNMC-B8D-T2 | — |
| 1.9 V± 2.0% | 0.095V | S-80819CNNB-B8E-T2 | S-80819CNY-X | S-80819CNUA-B8E-T2 | S-80819CNMC-B8E-T2 | — |
| 2.0 V± 2.0% | 0.100V | S-80820CNNB-B8F-T2 | S-80820CNY-X | S-80820CNUA-B8F-T2 | S-80820CNMC-B8F-T2 | — |
| 2.1 V± 2.0% | 0.105V | S-80821CNNB-B8G-T2 | S-80821CNY-X | S-80821CNUA-B8G-T2 | S-80821CNMC-B8G-T2 | — |
| 2.2 V± 2.0% | 0.110V | S-80822CNNB-B8H-T2 | S-80822CNY-X | S-80822CNUA-B8H-T2 | S-80822CNMC-B8H-T2 | — |
| 2.3 V± 2.0% | 0.115V | S-80823CNNB-B8I-T2 | S-80823CNY-X | S-80823CNUA-B8I-T2 | S-80823CNMC-B8I-T2 | — |
| 2.4 V± 2.0% | 0.120V | S-80824CNNB-B8J-T2 | S-80824CNY-X | S-80824CNUA-B8J-T2 | S-80824CNMC-B8J-T2 | — |
| 2.4 V typ. | 4.4±0.1V | — | S-80824KNY-X | S-80824KNUA-D2B-T2 | — | — |
| 2.5 V± 2.0% | 0.125V | S-80825CNNB-B8K-T2 | S-80825CNY-X | S-80825CNUA-B8K-T2 | S-80825CNMC-B8K-T2 | — |
| 2.6 V± 2.0% | 0.130V | S-80826CNNB-B8L-T2 | S-80826CNY-X | S-80826CNUA-B8L-T2 | — | — |
| 2.7 V± 2.0% | 0.135V | S-80827CNNB-B8M-T2 | S-80827CNY-X | S-80827CNUA-B8M-T2 | S-80827CNMC-B8M-T2 | S-80827CNBB-B8M-TF |
| 2.8 V± 2.0% | 0.140V | S-80828CNNB-B8N-T2 | S-80828CNY-X | S-80828CNUA-B8N-T2 | S-80828CNMC-B8N-T2 | — |
| 2.9 V± 2.0% | 0.145V | S-80829CNNB-B8O-T2 | S-80829CNY-X | S-80829CNUA-B8O-T2 | — | — |
| 3.0 V± 2.0% | 0.150V | S-80830CNNB-B8P-T2 | S-80830CNY-X | S-80830CNUA-B8P-T2 | S-80830CNMC-B8P-T2 | — |
| 3.1 V± 2.0% | 0.155V | S-80831CNNB-B8Q-T2 | S-80831CNY-X | S-80831CNUA-B8Q-T2 | — | — |
| 3.2 V± 2.0% | 0.160V | S-80832CNNB-B8R-T2 | S-80832CNY-X | S-80832CNUA-B8R-T2 | S-80832CNMC-B8R-T2 | — |
| 3.3 V± 2.0% | 0.165V | S-80833CNNB-B8S-T2 | S-80833CNY-X | S-80833CNUA-B8S-T2 | S-80833CNMC-B8S-T2 | — |
| 3.4 V± 2.0% | 0.170V | S-80834CNNB-B8T-T2 | S-80834CNY-X | S-80834CNUA-B8T-T2 | S-80834CNMC-B8T-T2 | — |
| 3.5 V± 2.0% | 0.175V | S-80835CNNB-B8U-T2 | S-80835CNY-X | S-80835CNUA-B8U-T2 | S-80835CNMC-B8U-T2 | — |
| 3.6 V± 2.0% | 0.180V | S-80836CNNB-B8V-T2 | S-80836CNY-X | S-80836CNUA-B8V-T2 | S-80836CNMC-B8V-T2 | — |
| 3.7 V± 2.0% | 0.185V | S-80837CNNB-B8W-T2 | S-80837CNY-X | S-80837CNUA-B8W-T2 | — | — |
| 3.8 V± 2.0% | 0.190V | S-80838CNNB-B8X-T2 | S-80838CNY-X | S-80838CNUA-B8X-T2 | — | — |
| 3.9 V± 2.0% | 0.195V | S-80839CNNB-B8Y-T2 | S-80839CNY-X | S-80839CNUA-B8Y-T2 | S-80839CNMC-B8Y-T2 | — |
| 4.0 V± 2.0% | 0.200V | S-80840CNNB-B8Z-T2 | S-80840CNY-X | S-80840CNUA-B8Z-T2 | S-80840CNMC-B8Z-T2 | — |
| 4.1 V± 2.0% | 0.205V | S-80841CNNB-B82-T2 | S-80841CNY-X | S-80841CNUA-B82-T2 | — | — |
| 4.2 V± 2.0% | 0.210V | S-80842CNNB-B83-T2 | S-80842CNY-X | S-80842CNUA-B83-T2 | S-80842CNMC-B83-T2 | — |
| 4.3 V± 2.0% | 0.215V | S-80843CNNB-B84-T2 | S-80843CNY-X | S-80843CNUA-B84-T2 | — | — |
| 4.4 V± 2.0% | 0.220V | S-80844CNNB-B85-T2 | S-80844CNY-X | S-80844CNUA-B85-T2 | S-80844CNMC-B85-T2 | — |
| 4.5 V± 2.0% | 0.225V | S-80845CNNB-B86-T2 | S-80845CNY-X | S-80845CNUA-B86-T2 | S-80845CNMC-B86-T2 | S-80845CNBB-B86-TF |
| 4.6 V± 2.0% | 0.230V | S-80846CNNB-B87-T2 | S-80846CNY-X | S-80846CNUA-B87-T2 | — | — |
| 4.6 V± 0.10V | 0.10V max. | — | S-80846KNY-X | S-80846KNUA-D2C-T2 | — | — |
| 4.7 V± 2.0% | 0.235V | S-80847CNNB-B88-T2 | S-80847CNY-X | S-80847CNUA-B88-T2 | — | — |
| 4.8 V± 2.0% | 0.240V | S-80848CNNB-B89-T2 | S-80848CNY-X | S-80848CNUA-B89-T2 | — | — |
| 4.9 V± 2.0% | 0.245V | S-80849CNNB-B9A-T2 | S-80849CNY-X | S-80849CNUA-B9A-T2 | — | — |
| 5.0 V± 2.0% | 0.250V | S-80850CNNB-B9B-T2 | S-80850CNY-X | S-80850CNUA-B9B-T2 | S-80850CNMC-B9B-T2 | — |
| 5.1 V± 2.0% | 0.255V | S-80851CNNB-B9C-T2 | S-80851CNY-X | S-80851CNUA-B9C-T2 | S-80851CNMC-B9C-T2 | — |
| 5.2 V± 2.0% | 0.260V | S-80852CNNB-B9D-T2 | — | S-80852CNUA-B9D-T2 | — | — |
| 5.3 V± 2.0% | 0.265V | S-80853CNNB-B9E-T2 | S-80853CNY-X | — | — | — |
| 5.4 V± 2.0% | 0.270V | S-80854CNNB-B9F-T2 | — | — | — | — |
| 5.5 V± 2.0% | 0.275V | S-80855CNNB-B9G-T2 | — | — | — | — |
| 5.6 V± 2.0% | 0.280V | S-80856CNNB-B9H-T2 | — | — | — | — |
| 5.7 V± 2.0% | 0.285V | S-80857CNNB-B9I-T2 | — | — | — | — |
| 5.8 V± 2.0% | 0.290V | S-80858CNNB-B9J-T2 | — | — | — | — |
| 5.9 V± 2.0% | 0.295V | S-80859CNNB-B9K-T2 | — | — | — | — |
| 6.0 V± 2.0% | 0.300V | S-80860CNNB-B9L-T2 | — | S-80860CNUA-B9L-T2 | — | — |

*: X changes according to the packing form in TO-92. Standard forms are B; Bulk and Z; Zigzag (tape and ammo).
If tape and reel (T) is needed, please contact SII sales office.

**Table 7 Selection Guide**

(2/2)

| Detection voltage range | Hysterisis (typ.) | CMOS (Active low) | | | | |
|---|---|---|---|---|---|---|
| | | SC-82AB | TO-92* | SOT-89-3 | SOT-23-5 | SNB(B) |
| 1.5 V± 2.0% | 0.075V | S-80815CLNB-B6A-T2 | S-80815CLY-X | S-80815CLUA-B6A-T2 | S-80815CLMC-B6A-T2 | — |
| 1.6 V± 2.0% | 0.080V | S-80816CLNB-B6B-T2 | S-80816CLY-X | S-80816CLUA-B6B-T2 | — | — |
| 1.7 V± 2.0% | 0.085V | S-80817CLNB-B6C-T2 | S-80817CLY-X | S-80817CLUA-B6C-T2 | — | — |
| 1.8 V± 2.0% | 0.090V | S-80818CLNB-B6D-T2 | S-80818CLY-X | S-80818CLUA-B6D-T2 | S-80818CLMC-B6D-T2 | — |
| 1.9 V± 2.0% | 0.095V | S-80819CLNB-B6E-T2 | S-80819CLY-X | S-80819CLUA-B6E-T2 | S-80819CLMC-B6E-T2 | — |
| 2.0 V± 2.0% | 0.100V | S-80820CLNB-B6F-T2 | S-80820CLY-X | S-80820CLUA-B6F-T2 | S-80820CLMC-B6F-T2 | — |
| 2.1 V± 2.0% | 0.105V | S-80821CLNB-B6G-T2 | S-80821CLY-X | S-80821CLUA-B6G-T2 | S-80821CLMC-B6G-T2 | — |
| 2.2 V± 2.0% | 0.110V | S-80822CLNB-B6H-T2 | S-80822CLY-X | S-80822CLUA-B6H-T2 | — | — |
| 2.3 V± 2.0% | 0.115V | S-80823CLNB-B6I-T2 | S-80823CLY-X | S-80823CLUA-B6I-T2 | S-80823CLMC-B6I-T2 | — |
| 2.4 V± 2.0% | 0.120V | S-80824CLNB-B6J-T2 | S-80824CLY-X | S-80824CLUA-B6J-T2 | — | — |
| 2.5 V± 2.0% | 0.125V | S-80825CLNB-B6K-T2 | S-80825CLY-X | S-80825CLUA-B6K-T2 | S-80825CLMC-B6K-T2 | — |
| 2.6 V± 2.0% | 0.130V | S-80826CLNB-B6L-T2 | S-80826CLY-X | S-80826CLUA-B6L-T2 | — | — |
| 2.7 V± 2.0% | 0.135V | S-80827CLNB-B6M-T2 | S-80827CLY-X | S-80827CLUA-B6M-T2 | S-80827CLMC-B6M-T2 | S-80827CLBB-B6M-TF |
| 2.8 V± 2.0% | 0.140 | S-80828CLNB-B6N-T2 | S-80828CLY-X | S-80828CLUA-B6N-T2 | S-80828CLMC-B6N-T2 | — |
| 2.9 V± 2.0% | 0.145V | S-80829CLNB-B6O-T2 | S-80829CLY-X | S-80829CLUA-B6O-T2 | — | — |
| 3.0 V± 2.0% | 0.150V | S-80830CLNB-B6P-T2 | S-80830CLY-X | S-80830CLUA-B6P-T2 | S-80830CLMC-B6P-T2 | — |
| 3.1 V± 2.0% | 0.155V | S-80831CLNB-B6Q-T2 | S-80831CLY-X | S-80831CLUA-B6Q-T2 | — | — |
| 3.2 V± 2.0% | 0.160V | S-80832CLNB-B6R-T2 | S-80832CLY-X | S-80832CLUA-B6R-T2 | S-80832CLMC-B6R-T2 | — |
| 3.3 V± 2.0% | 0.165V | S-80833CLNB-B6S-T2 | S-80833CLY-X | S-80833CLUA-B6S-T2 | S-80833CLMC-B6S-T2 | — |
| 3.4 V± 2.0% | 0.170V | S-80834CLNB-B6T-T2 | S-80834CLY-X | S-80834CLUA-B6T-T2 | — | — |
| 3.5 V± 2.0% | 0.175V | S-80835CLNB-B6U-T2 | S-80835CLY-X | S-80835CLUA-B6U-T2 | S-80835CLMC-B6U-T2 | — |
| 3.6 V± 2.0% | 0.180V | S-80836CLNB-B6V-T2 | S-80836CLY-X | S-80836CLUA-B6V-T2 | — | — |
| 3.7 V± 2.0% | 0.185V | S-80837CLNB-B6W-T2 | S-80837CLY-X | S-80837CLUA-B6W-T2 | — | — |
| 3.8 V± 2.0% | 0.190V | S-80838CLNB-B6X-T2 | S-80838CLY-X | S-80838CLUA-B6X-T2 | — | — |
| 3.9 V± 2.0% | 0.195V | S-80839CLNB-B6Y-T2 | S-80839CLY-X | S-80839CLUA-B6Y-T2 | — | — |
| 4.0 V± 2.0% | 0.200V | S-80840CLNB-B6Z-T2 | S-80840CLY-X | S-80840CLUA-B6Z-T2 | S-80840CLMC-B6Z-T2 | — |
| 4.1 V± 2.0% | 0.205V | S-80841CLNB-B62-T2 | S-80841CLY-X | S-80841CLUA-B62-T2 | — | — |
| 4.2 V± 2.0% | 0.210V | S-80842CLNB-B63-T2 | S-80842CLY-X | S-80842CLUA-B63-T2 | S-80842CLMC-B63-T2 | — |
| 4.3 V± 2.0% | 0.215V | S-80843CLNB-B64-T2 | S-80843CLY-X | S-80843CLUA-B64-T2 | — | — |
| 4.4 V± 2.0% | 0.220V | S-80844CLNB-B65-T2 | S-80844CLY-X | S-80844CLUA-B65-T2 | — | — |
| 4.45 V typ. | 4.70V max. | — | S-80844KLY-X | S-80844KLUA-D2A-T2 | — | — |
| 4.5 V± 2.0% | 0.225V | S-80845CLNB-B66-T2 | S-80845CLY-X | S-80845CLUA-B66-T2 | S-80845CLMC-B66-T2 | S-80845CLBB-B66-TF |
| 4.6 V± 2.0% | 0.230V | S-80846CLNB-B67-T2 | S-80846CLY-X | S-80846CLUA-B67-T2 | — | — |
| 4.7 V± 2.0% | 0.235V | S-80847CLNB-B68-T2 | S-80847CLY-X | S-80847CLUA-B68-T2 | — | — |
| 4.8 V± 2.0% | 0.240V | S-80848CLNB-B69-T2 | S-80848CLY-X | S-80848CLUA-B69-T2 | — | — |
| 4.9 V± 2.0% | 0.245V | S-80849CLNB-B7A-T2 | S-80849CLY-X | S-80849CLUA-B7A-T2 | S-80849CLMC-B7A-T2 | — |
| 5.0 V± 2.0% | 0.250V | S-80850CLNB-B7B-T2 | S-80850CLY-X | S-80850CLUA-B7B-T2 | S-80850CLMC-B7B-T2 | — |
| 5.1 V± 2.0% | 0.255V | S-80851CLNB-B7C-T2 | S-80851CLY-X | S-80851CLUA-B7C-T2 | S-80851CLMC-B7C-T2 | — |
| 5.2 V± 2.0% | 0.260V | S-80852CLNB-B7D-T2 | — | S-80852CLUA-B7D-T2 | S-80852CLMC-B7D-T2 | — |
| 5.3 V± 2.0% | 0.265V | S-80853CLNB-B7E-T2 | — | — | — | — |
| 5.4 V± 2.0% | 0.270V | S-80854CLNB-B7F-T2 | — | — | — | — |
| 5.5 V± 2.0% | 0.275V | S-80855CLNB-B7G-T2 | — | S-80855CLUA-B7G-T2 | — | — |
| 5.6 V± 2.0% | 0.280V | S-80856CLNB-B7H-T2 | — | — | — | — |
| 5.7 V± 2.0% | 0.285V | S-80857CLNB-B7I-T2 | — | — | — | — |
| 5.8 V± 2.0% | 0.290V | S-80858CLNB-B7J-T2 | — | — | — | — |
| 5.9 V± 2.0% | 0.295V | S-80859CLNB-B7K-T2 | — | — | — | — |
| 6.0 V± 2.0% | 0.300V | S-80860CLNB-B7L-T2 | — | — | — | — |

*: X changes according to the packing form in TO-92. Standard forms are B; Bulk and Z; Zigzag (tape and ammo). If tape and reel (T) is needed, please contact SII sales office.

## ■ Output Forms

1. Output forms in S-808xxC Series

| | Nch open-drain (Active low) | CMOS output (Active low) |
|---|---|---|
| S-808xxC Series | "N" is the last letter of the model number. e.g. S-80815CN | "L" is the last letter of the model number e.g. S-80815CL |

2. Output forms and their usage

| Usage | Nch ("L") | CMOS ("L") |
|---|---|---|
| Different power supplies | Yes | No |
| Active low reset for CPUs | Yes | Yes |
| Active high reset for CPUs | No | No |
| Detection voltage change by resistor divider | Yes | No |

✶Example for two power supplies ✶Example for one power supply

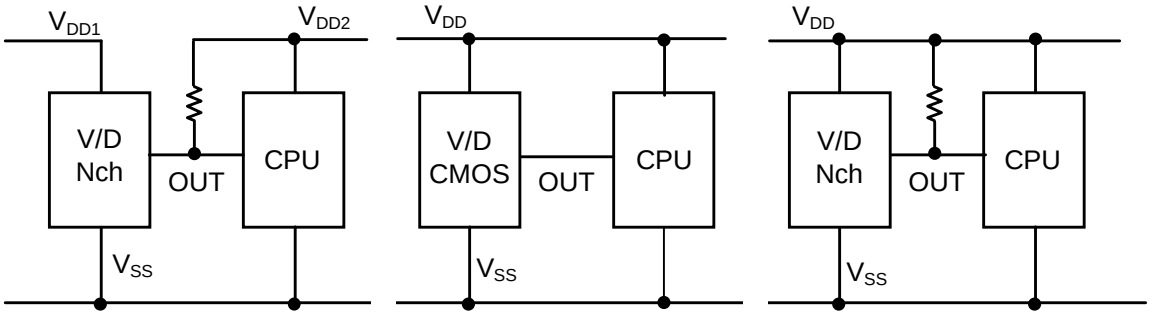



Figure 7

## ■ Absolute Maximum Ratings

**Table 8 Absolute Maximum Ratings**

(Ta=25°C, Unless otherwise specified)

| Parameter | | Symbol | | Rarings | Unit |
|---|---|---|---|---|---|
| Power supply voltage | | $V_{DD}$-$V_{SS}$ | | 12 | V |
| Output voltage | Nch open-drain | $V_{OUT}$ | | $V_{SS}$-0.3 to 12 | V |
| | CMOS | | | $V_{SS}$-0.3 to $V_{DD}$+0.3 | V |
| Output current | | $I_{OUT}$ | | 50 | mA |
| Power dissipation | | $P_D$ | TO-92 | 400 | mW |
| | | | SOT-89-3 | 500 | |
| | | | SC-82AB, SOT-23-5 | 150 | |
| | | | SNB(B) | 60 | |
| Operating temperature | | $T_{opr}$ | | -40 to +85 | °C |
| Storage temperature | | $T_{stg}$ | | -40 to +125 | °C |

Note: Although the IC contains protection circuit against static electricity, excessive static electricity or voltage which exceeds the limit of the protection circuit should not be applied to.

## ■ Electrical Characteristics

1.Standard products

**Table 9 Electrical Characteristics**

(Ta=25 °C, Unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units | Test circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage | $-V_{DET}$ | — | | $-V_{DET}$ ×0.98 | $-V_{DET}$ | $-V_{DET}$ ×1.02 | V | 1 |
| Hysteresis width | $V_{HYS}$ | — | | $-V_{DET}$ ×0.03 | $-V_{DET}$ ×0.05 | $-V_{DET}$ ×0.08 | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD}$=3.5V | S-80815 ~ 26 | — | 0.8 | 2.4 | µA | 2 |
| | | $V_{DD}$=4.5V | S-80827 ~ 39 | — | 0.8 | 2.4 | | |
| | | $V_{DD}$=6.0V | S-80840 ~ 56 | — | 0.9 | 2.7 | | |
| | | $V_{DD}$=7.5V | S-80857 ~ 60 | — | 0.9 | 2.7 | | |
| Operating voltage | $V_{DD}$ | — | | 0.95 | — | 10.0 | V | 1 |
| Output current of output transistor | $I_{OUT}$ | Nch<br>$V_{OUT}$=0.5V | $V_{DD}$=1.2V S-80815 ~ 26 | 0.23 | 0.50 | — | mA | 3 |
| | | | $V_{DD}$=2.4V S-80827 ~ 60 | 1.60 | 3.70 | — | | |
| | | Pch<br>(applied for CMOS output products)<br>$V_{OUT}$=$V_{DD}$ - 0.5V | $V_{DD}$=4.8V S-80815 ~ 39 | 0.36 | 0.62 | — | | 4 |
| | | | $V_{DD}$=6.0V S-80840 ~ 56 | 0.46 | 0.75 | — | | |
| | | | $V_{DD}$=8.4V S-80857 ~ 60 | 0.59 | 0.96 | — | | |
| Leakage current of output transistor | $I_{LEAK}$ | Nch<br>(applied for Nch open-drain output products)<br>$V_{OUT}$=10.0V, $V_{DD}$=10.0V | | — | — | 0.1 | µA | 3 |
| Response time | tPLH | | | — | — | 60 | µs | 1 |
| Temperature [1] coefficient for detection voltage | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -VDET}$ | Ta=–40°C to +85°C | | — | 100 | 350 | ppm/°C | 1 |

1) Temperature change ratio for the detection voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[mV/°C] = -V_{DET}[V] \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[ppm/°C] \div 1000$$

Specified detection voltage

Temperature coefficient for detection voltage

Temperature change ratio for detection voltage

2) Customized products
S-80824KNUA-D2B-T2/S-80824KNY-X

**Table 10**

(Ta=25 °C, Unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units | Test circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage | $-V_{DET}$ | — | | 2.295 | 2.400 | 2.505 | V | 1 |
| Release voltage | $+V_{DET}$ | — | | 4.300 | 4.400 | 4.500 | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD}$=6.0V | | — | 1.0 | 3.0 | µA | 2 |
| Operating voltage | $V_{DD}$ | — | | 0.95 | — | 10.0 | V | 1 |
| Output current of output transistor | $I_{OUT}$ | Nch $V_{OUT}$=0.5V | $V_{DD}$=0.95V | 0.03 | 0.25 | — | mA | 3 |
| | | | $V_{DD}$=1.2V | 0.23 | 0.50 | — | mA | 4 |
| Leakage current of output transistor | $I_{LEAK}$ | Nch $V_{OUT}$=10.0V $V_{DD}$=10.0V | | — | — | 0.1 | µA | 3 |
| Response time | tPLH | — | | — | — | 60 | µs | 1 |
| Temperature [1] coefficient for detection voltage | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -VDET}$ | Ta=–40°C to +85°C | | — | 100 | 350 | ppm/°C | 1 |

S-80844KLUA-D2A-T2/S-80844KLY-X

**Table 11**

(Ta=25 °C, Unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units | Test circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage | $-V_{DET}$ | — | | 4.295 | 4.450 | 4.605 | V | 1 |
| Release voltage | $+V_{DET}$ | — | | — | — | 4.700 | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD}$=6.0V | | — | 1.0 | 3.0 | µA | 2 |
| Operating voltage | $V_{DD}$ | — | | 0.95 | — | 10.0 | V | 1 |
| Output current of output transistor | $I_{OUT}$ | Nch $V_{OUT}$=0.5V | $V_{DD}$=1.2V | 0.23 | 0.50 | — | mA | 3 |
| | | | $V_{DD}$=2.4V | 1.60 | 3.70 | — | | |
| | | Pch $V_{OUT}$ = $V_{DD}$ - 0.5V | $V_{DD}$=4.8V | 0.36 | 0.62 | — | mA | 4 |
| Response time | tPLH | — | | — | — | 60 | µs | 1 |
| Temperature [1] coefficient for detection voltage | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -VDET}$ | Ta=–40°C to +85°C | | — | 100 | 350 | ppm/°C | 1 |

S-80846KNUA-D2C-T2/S-80846KNY-X

**Table 12**

(Ta=25 °C, Unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units | Test circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage | $-V_{DET}$ | — | | 4.500 | 4.600 | 4.700 | V | 1 |
| Hysteresis width | $V_{HYS}$ | — | | — | 0.05 | 0.10 | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD}$=6.0V | | — | 1.0 | 3.0 | µA | 2 |
| Operating voltage | $V_{DD}$ | — | | 0.95 | — | 10.0 | V | 1 |
| Output current of output transistor | $I_{OUT}$ | Nch $V_{OUT}$=0.5V | $V_{DD}$=1.2V | 0.23 | 0.50 | — | mA | 3 |
| | | | $V_{DD}$=2.4V | 1.60 | 3.70 | — | mA | 4 |
| Leakage current of output transistor | $I_{LEAK}$ | Nch $V_{DD}$=10.0V $V_{OUT}$=10.0V | | — | — | 0.1 | µA | 3 |
| Response time | tPLH | — | | — | — | 60 | µs | 1 |
| Temperature [1] coefficient for detection voltage | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -VDET}$ | Ta=–40°C to +85°C | | — | 100 | 350 | ppm/°C | 1 |

1) Temperature change ratio for the detection voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[mV/°C] = -V_{DET}[V] \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[ppm/°C] \div 1000$$

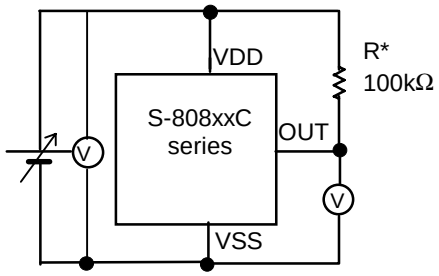
Specified detection voltage

Temperature coefficient for detection voltage

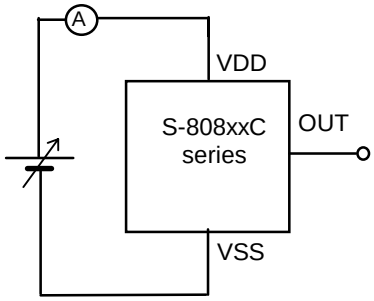
Temperature change ratio for detection voltage

## ■ Test Circuits

1.

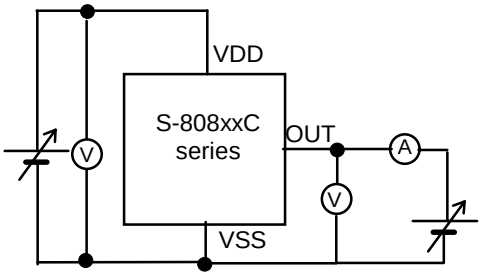



2.




* R is unnecessary for CMOS output products.

3.




4.

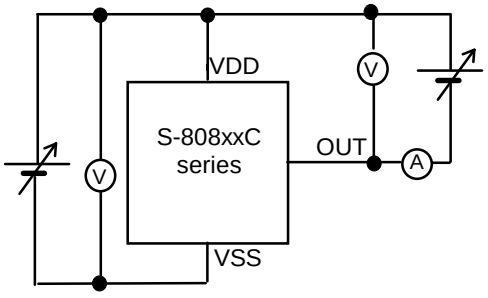



**Figure 8 Test Circuits**

## ■ Definition of Terms

1. Detection voltage ($-V_{DET}$)

   Detection voltage ($-V_{DET}$) is a voltage at which the output turns to low. The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the minimum [($-V_{DET}$)min.] and the maximum [($-V_{DET}$)max.] is called the detection voltage range (See Figure 9).

   Example : For the S-80815CN, the detection voltage lies in the range of $1.470 \leq (-V_{DET}) \leq 1.530$.
   This means that some S-80815CNs have 1.470V for $-V_{DET}$ and some have 1.530V.

2. Release voltage ($+V_{DET}$)

   Release voltage ($+V_{DET}$) is a voltage at which the output turns to high. The release voltage varies slightly among products of the same specification. The variation of release voltages between the minimum [($+V_{DET}$)min.] and the maximum [($+V_{DET}$)max.] is called the release voltage range (See Figure 10).

   Example : For the S-80815CN, the release voltage lies in the range of $1.514 \leq (+V_{DET}) \leq 1.652$.
   This means that some S-80815CNs have 1.514V for $+V_{DET}$ and some have 1.652V.

   Remark: Although the detection voltage and release voltage overlap in the range of 1.514 V to 1.530 V, $+V_{DET}$ is always larger than $-V_{DET}$.

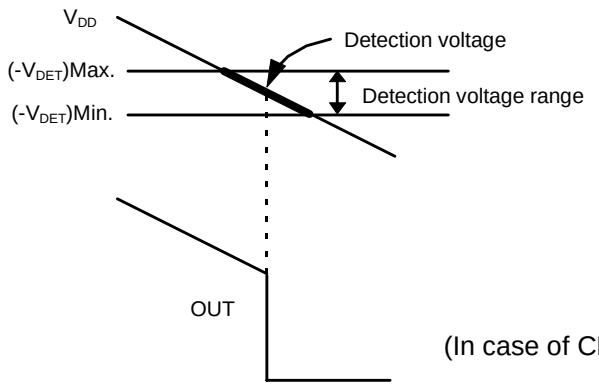
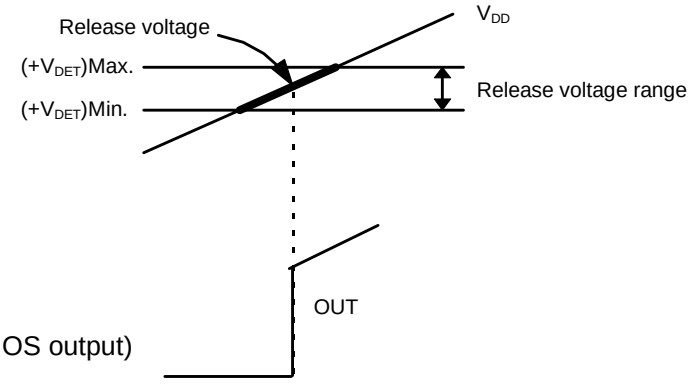



**Figure 9 Detection Voltage**




(In case of CMOS output)

**Figure 10 Release Voltage**

3. Hysteresis width ($V_{HYS}$)

   Hysteresis width is the voltage difference between the detection voltage and the release voltage. The existence of the hysteresis width avoids malfunction caused by noise on input signal.

4. Short-circuit current

   Short-circuit current in a voltage detector is the current which flows instantaneously at the time of detection and release of a voltage detector. The short-circuit current is large in CMOS out put products, small in Nch open-drain output products.

5. Oscillation

In applications where a resistor is connected to the voltage detector input (Figure 11), taking a CMOS active low product for example, the short-circuit current which is generated when the output goes from low to high (release) causes a voltage drop equal to [short-circuit current] × [input resistance] across the resistor. When the input voltage falls below the detection voltage $-V_{DET}$ as a result, the output voltage goes to low level. In this state, the short-circuit current stops and its resultant voltage drop disappears, and the output goes from low to high. Short-circuit current is again generated, a voltage drop appears, and oscillation is finally induced by repeating the process.

Following is an example for bad implementation: input voltage divider for a CMOS output product.

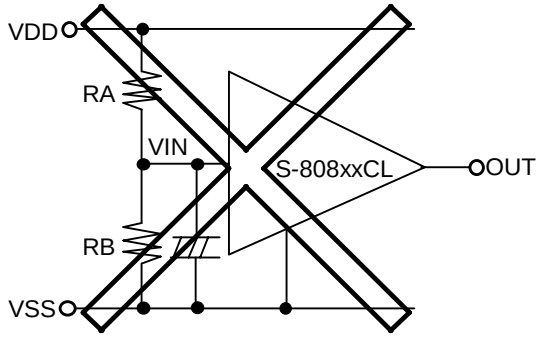



**Figure 11 An example for bad implementation**

## ■ Standard Circuit

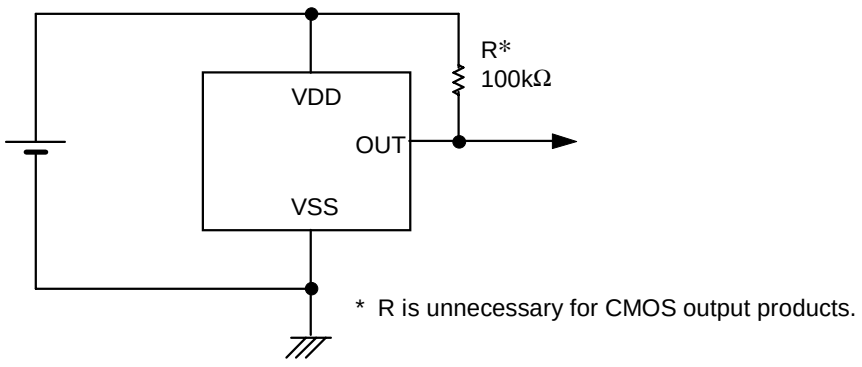



**Figure 12 Standard Circuit**

## ■ Operation Description

1. Basic operation : In case of CMOS active low output

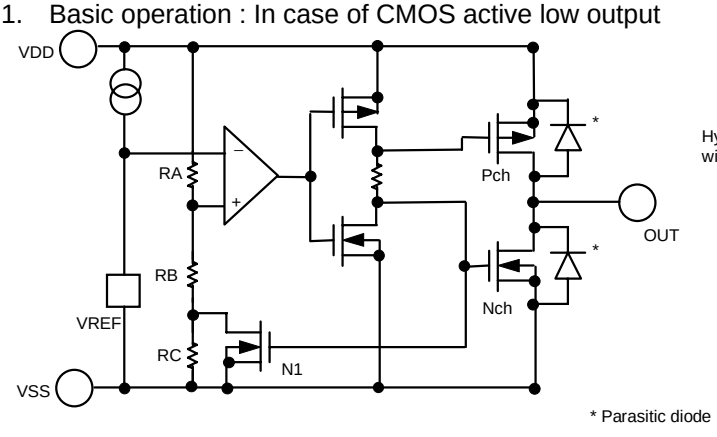



**Figure 13 Operation 1**

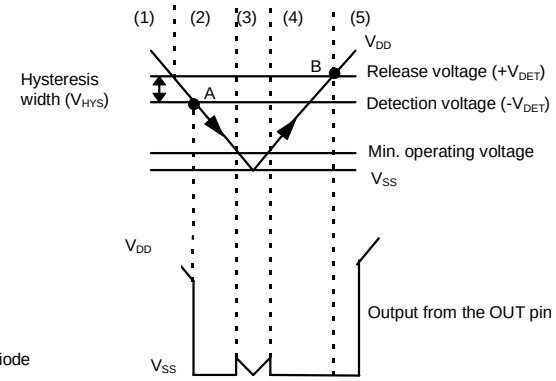



**Figure 14 Operation 2**

(1) When the power supply voltage $V_{DD}$ is higher than the release voltage $+V_{DET}$, the Nch transistor is OFF and the Pch transistor is ON to provide $V_{DD}$ (high) at the output. Since the Nch transistor N1 in Figure 13 is OFF, the comparator input voltage is $(RB+RC)/(RA+RB+RC)\times V_{DD}$.

(2) When the $V_{DD}$ goes below $+V_{DET}$, the output provides the $V_{DD}$ level, as long as the $V_{DD}$ remains above the detection voltage $-V_{DET}$. When the $V_{DD}$ falls below $-V_{DET}$ (point A in Figure 14), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the $V_{SS}$ level appears at the output. At this time the Nch transistor N1 in Figure 13 becomes ON, the comparator input voltage is changed to $RB/(RA+RB)\times V_{DD}$.

(3) When the $V_{DD}$ falls below the minimum operating voltage, the output becomes undefined, or goes to the $V_{DD}$ when the output is pulled up to the $V_{DD}$.

(4) The $V_{SS}$ level appears when the $V_{DD}$ rises above the minimum operating voltage. The $V_{SS}$ level still appears even when the $V_{DD}$ surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

(5) When the $V_{DD}$ rises above $+V_{DET}$ (point B in Figure 14), the Nch transistor becomes OFF and the Pch transistor becomes ON to provide $V_{DD}$ level at the output.

2. Other characteristics

(1) Temperature dependence of detection voltage

The temperature dependence of the detection voltage is shown by the shaded area in Figure 15.

S-80827C:

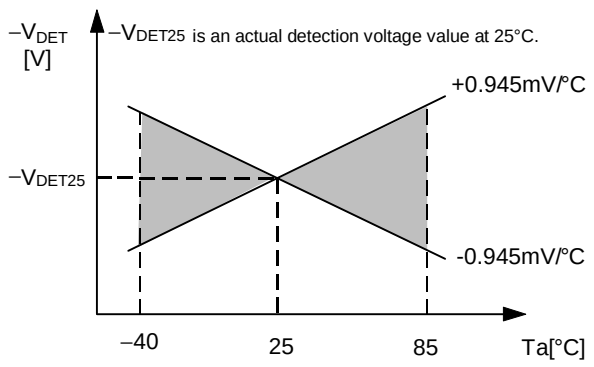



**Figure 15 Temperature dependence of Detection Voltage**

(2) Temperature dependence of release voltage

The temperature coefficient $\left(\frac{\Delta + V_{DET}}{\Delta Ta}\right)$ of the release voltage is calculated by the temperature coefficient $\left(\frac{\Delta - V_{DET}}{\Delta Ta}\right)$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

The temperature coefficients for the release voltage and the detection voltage have the same sign consequently.

(3) Temperature characteristics of hysteresis voltage

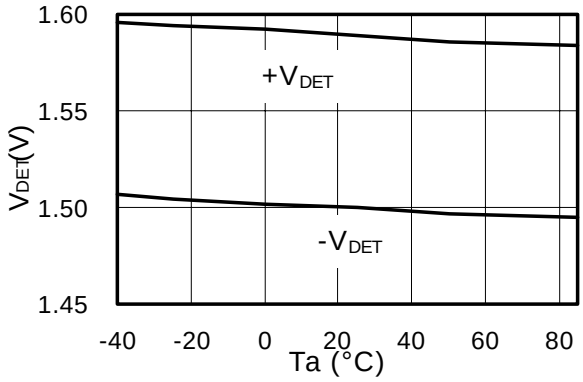
The temperature dependence of hysteresis voltage is expreseed as $\left(\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}\right)$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

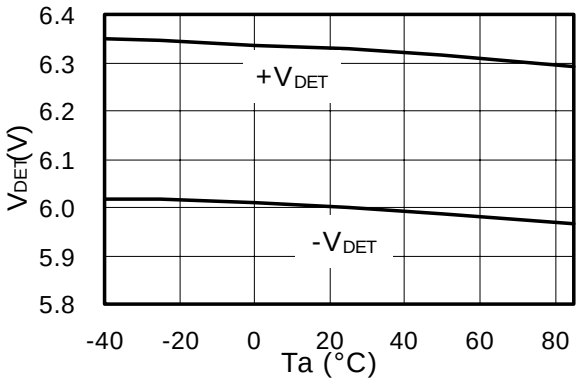
## ■ Typical Characteristics

(1) Detection voltage ($V_{DET}$) - Temperature (Ta)

S-80815CL

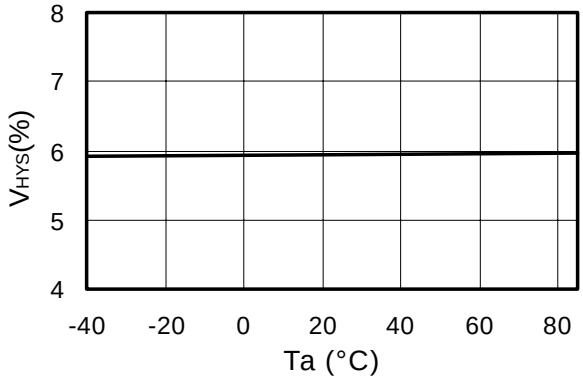



S-80860CL

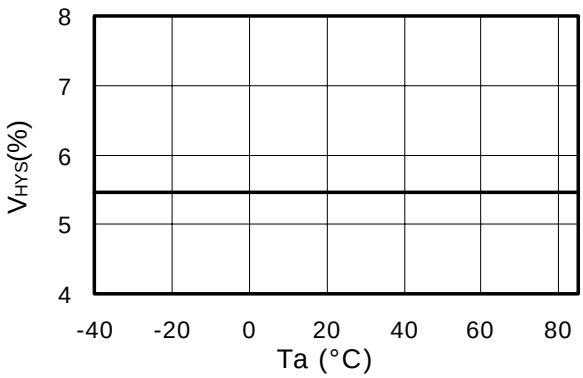



(2) Hysteresis voltage width ($V_{HYS}$) - Temperature (Ta)

S-80815CL

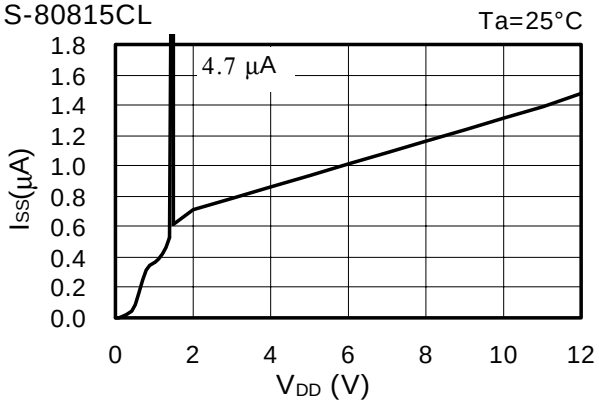



S-80860CL

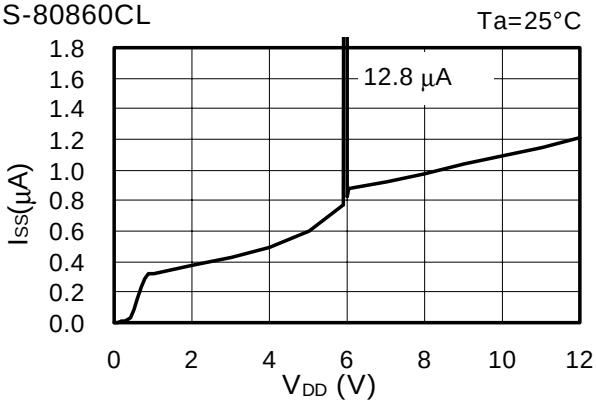



(3) Current consumption ($I_{SS}$) - Input voltage ($V_{DD}$)

S-80815CL

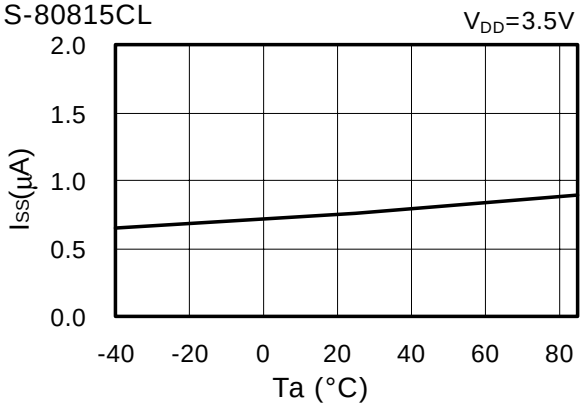



S-80860CL

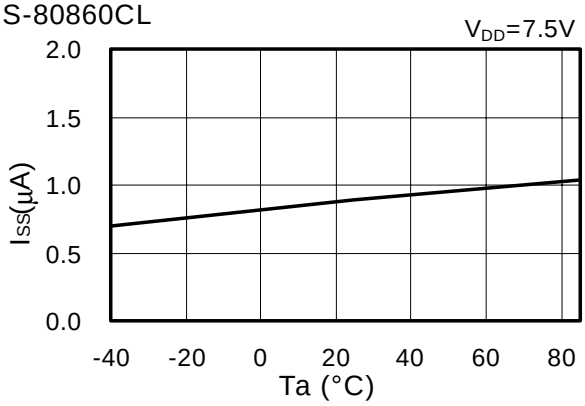



(4) Current consumption ($I_{SS}$) - Temperature (Ta)

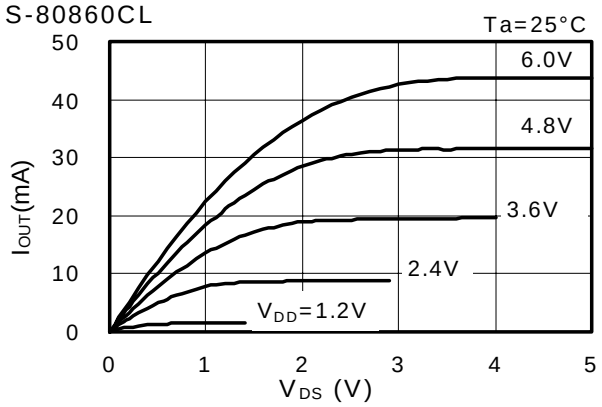
S-80815CL



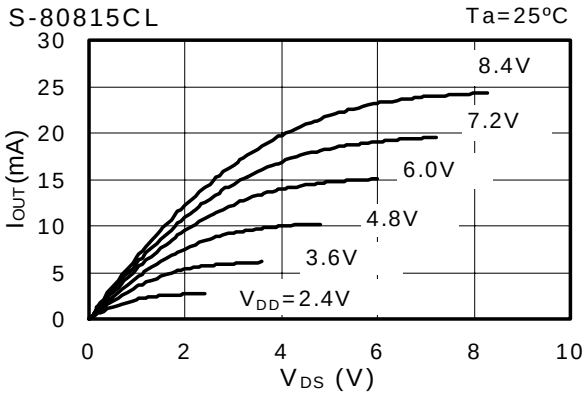

S-80860CL



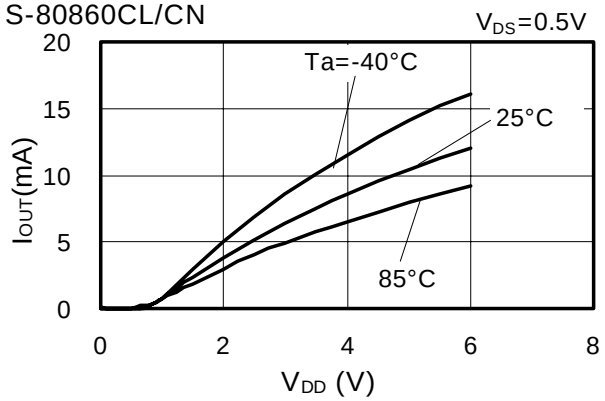
(5) Nch transistor output current ($I_{OUT}$) -$V_{DS}$



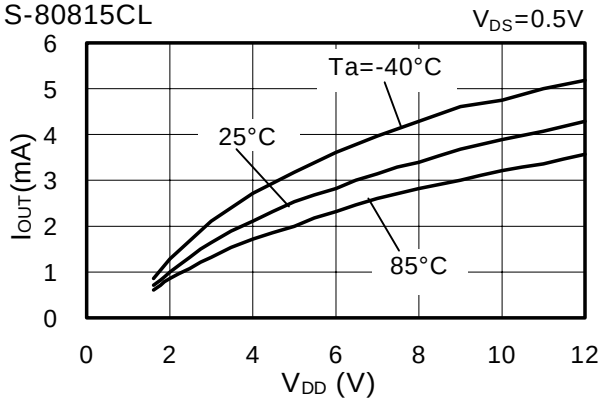

(6) Pch transistor output current ($I_{OUT}$) -$V_{DS}$



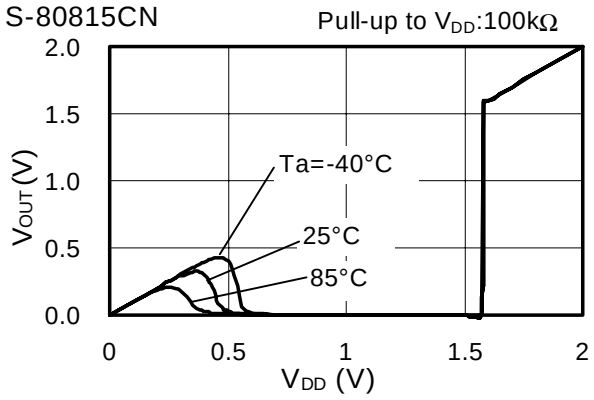

(7) Nch transistor output current ($I_{OUT}$)

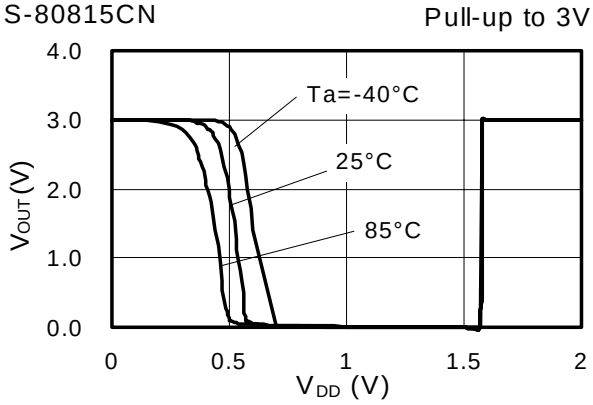


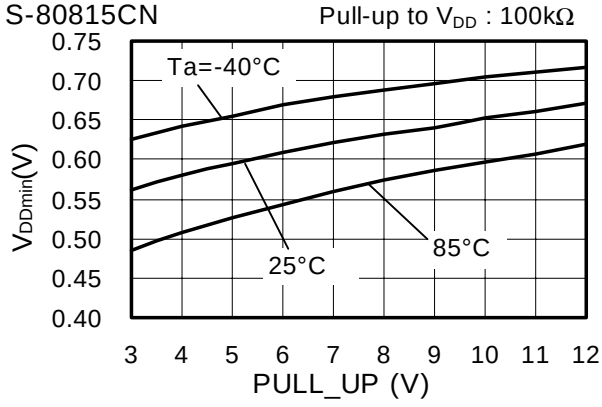

(8) Pch transistor output current ($I_{OUT}$)

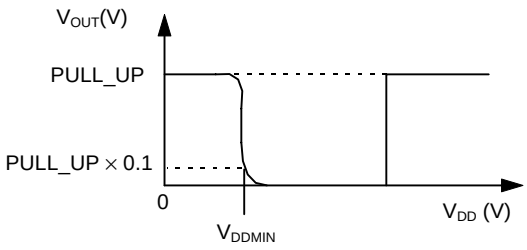



(9) Minimum operating voltage - Input voltage($V_{DD}$)



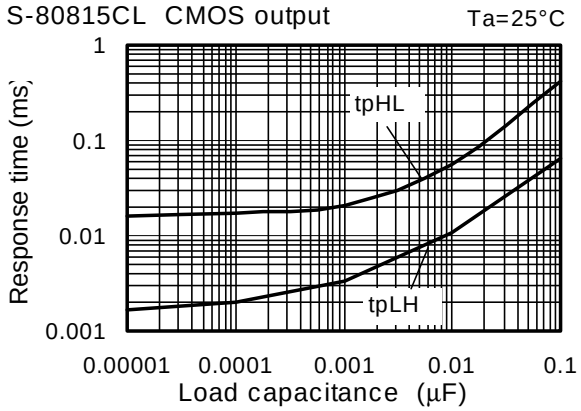



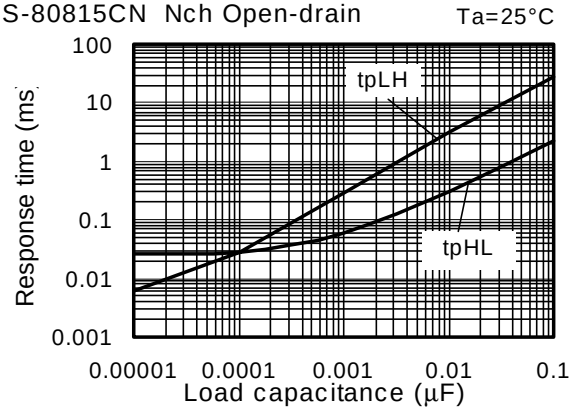



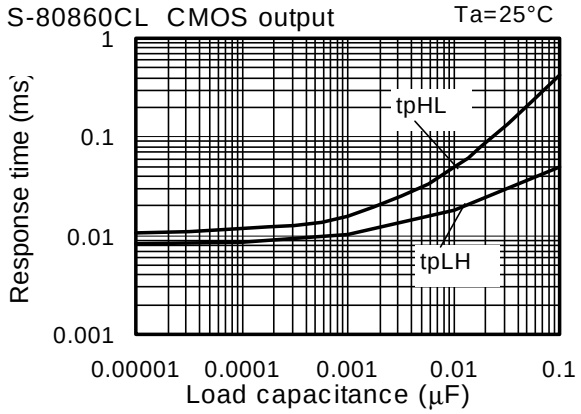

Note)

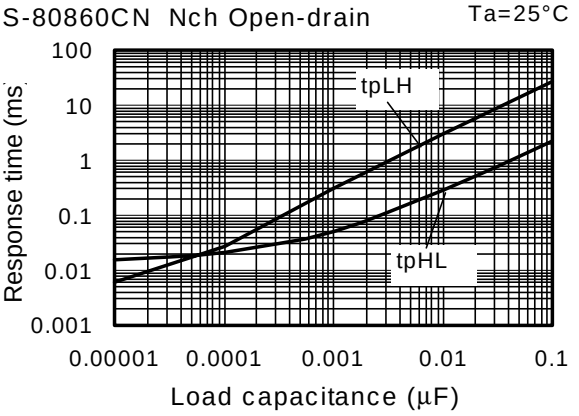
$V_{DDMIN.}$ Is defired by the $V_{DD}$ voltage at which $V_{OUT}$ is equal to the 10% of PULL-UP voltage when the $V_{DD}$ increase from 0V.

(10) Response time - Load capacitor ($C_{OUT}$)



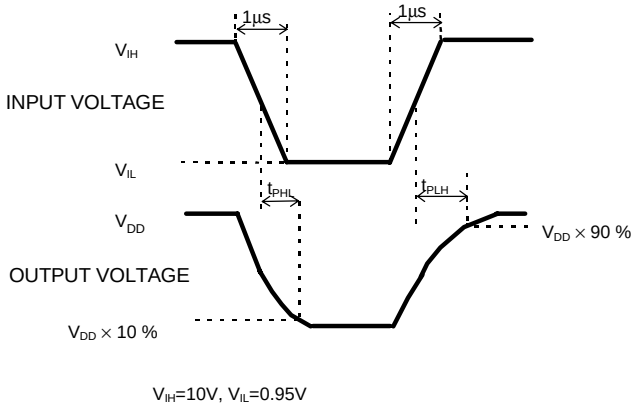
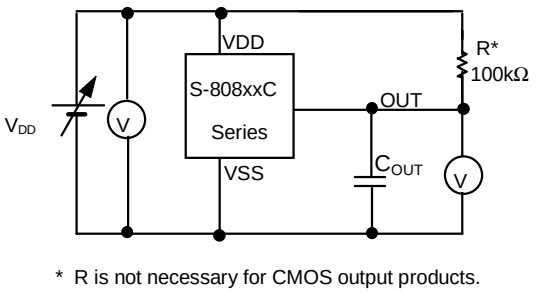




**Figure 16 Measurment Condition for Response Time**




* R is not necessary for CMOS output products.

**Figure 17 Measurment Circuit for Response Time**

## ■ Application Circuit Examples

1. Microcomputer reset circuits
   Reset circuits shown in figures 18 and 19 can be easily constructed with the help of the S-808xxC series, since the detector has low operating voltage, a high-precision detection voltage and hysteresis.

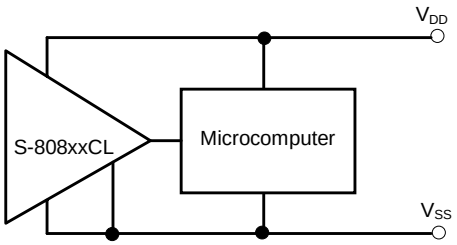
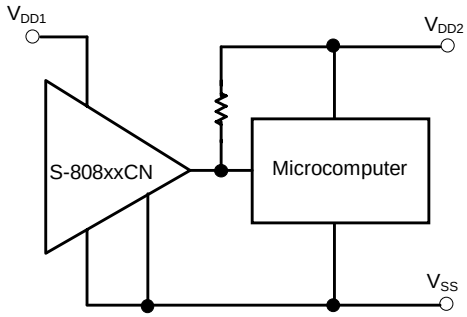



**Figure 18 Reset Circuit (S-808xxCL)**




(Nch open-drain output products only)

**Figure 19 Reset Circuit (S-808xxCN)**

2 Power-on reset circuit

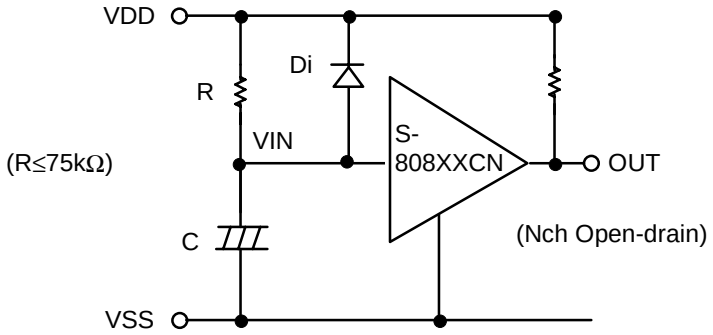



**Figure 20**

Note:1) Resistor R should be 75kΩ or less to avoid oscillation.
Note:2) Diode Di instantaneously discharges the charge stored in the capacitor C at the power falling, Di can be removed when the delay of the falling time is not important.

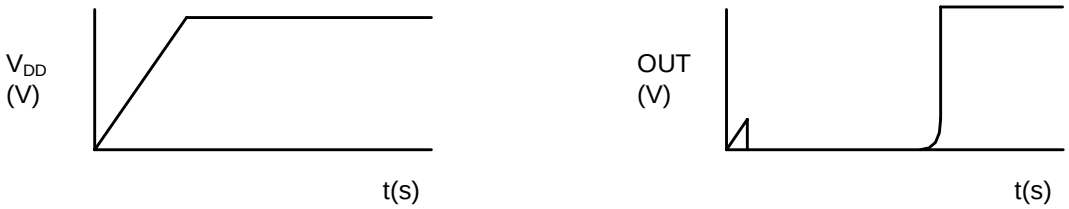


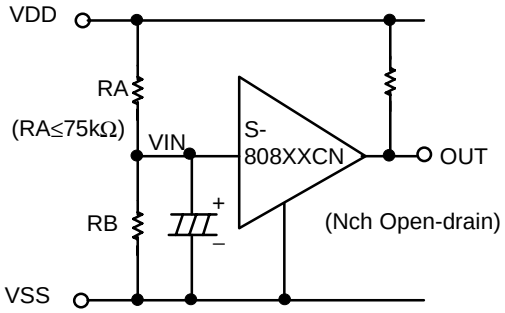

**Figure 21**

Note:3) When the power rises sharply as shown in the figure 22 left, the output may goes to the high level for an instant in the undefined region where the output voltage is undefined since the power voltage is less than the minimum operation voltage.


**Figure 22**

3. Change of detection voltage

In Nch open-drain output products of the S-808xxC series, detection voltage can be changed using resistance dividers or diodes as shown in figures 23 and 24. In figure 23 hysteresis width also changes.

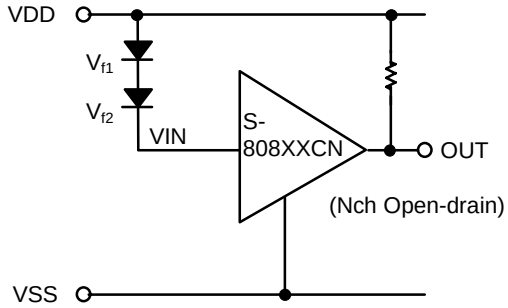



$$\text{Detection voltage} = \frac{RA+RB}{RB} \bullet -V_{DET}$$

$$\text{Hysterisis Width} = \frac{RA+RB}{RB} \bullet V_{HYS}$$

Note1: If RA and RB are large, the hysteresis width may be larger than the value given by the above equation due to the short-circuit current (which flows slightly in an Nch open-drain product).
Note2: RA should be 75kΩ or less to avoid oscillation.

Figure 23




Detection voltage=$V_{f1}+V_{f2}+(-V_{DET})$

Figure 24

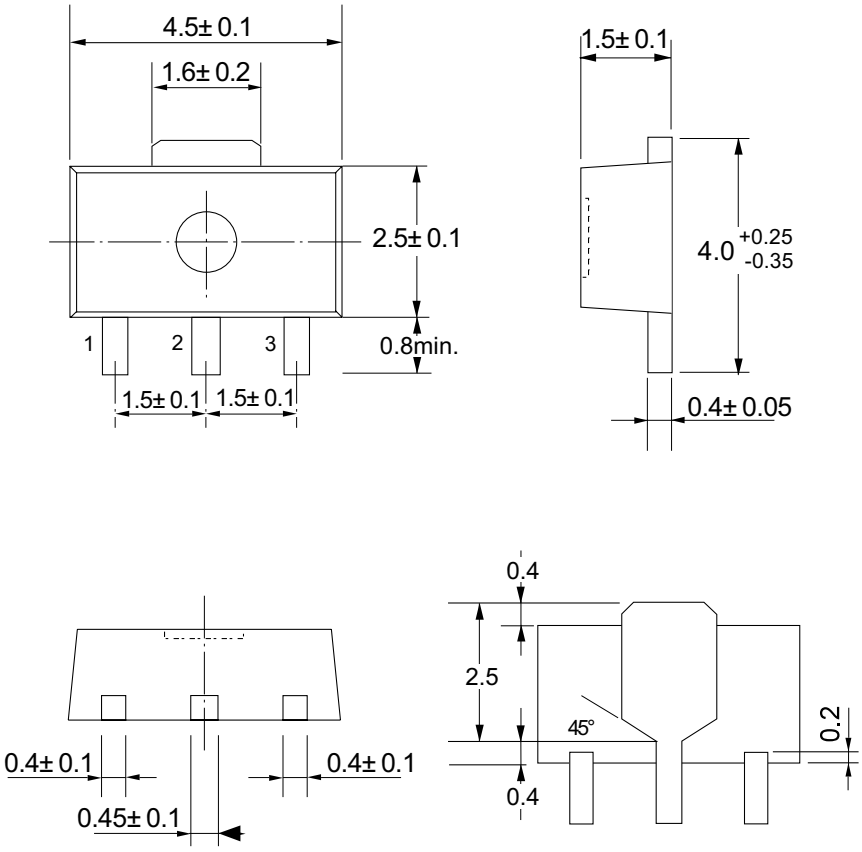
## ■ Notes

- In CMOS output products of the S-808xxC series, the short-circuit current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the short-circuit current during releasing.
- When designing for mass production using an application circuit described herein, parts deviation and temperature characteristics should be taken into consideration.
- Seiko Instruments Inc. shall not bear any responsibility for the patents on the circuits described herein.

# ■ SOT-89-3

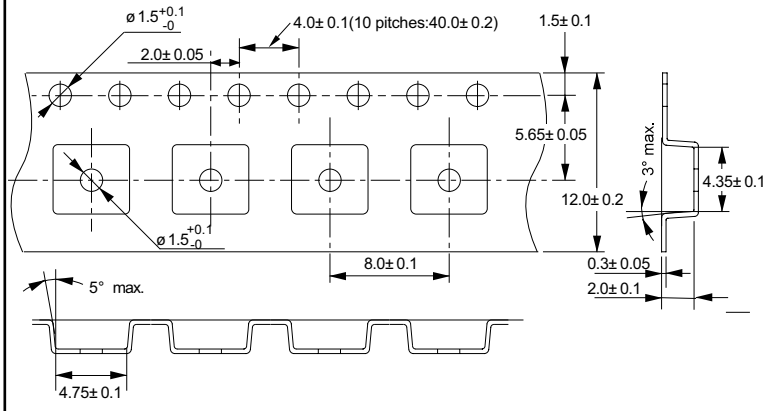
## ●Dimensions

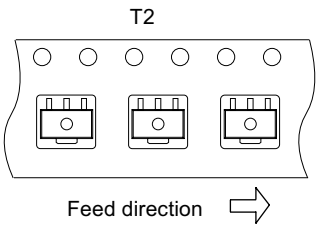
Unit:mm




No. UP003-A-P-SD-1.0

## ●Taping Specifications

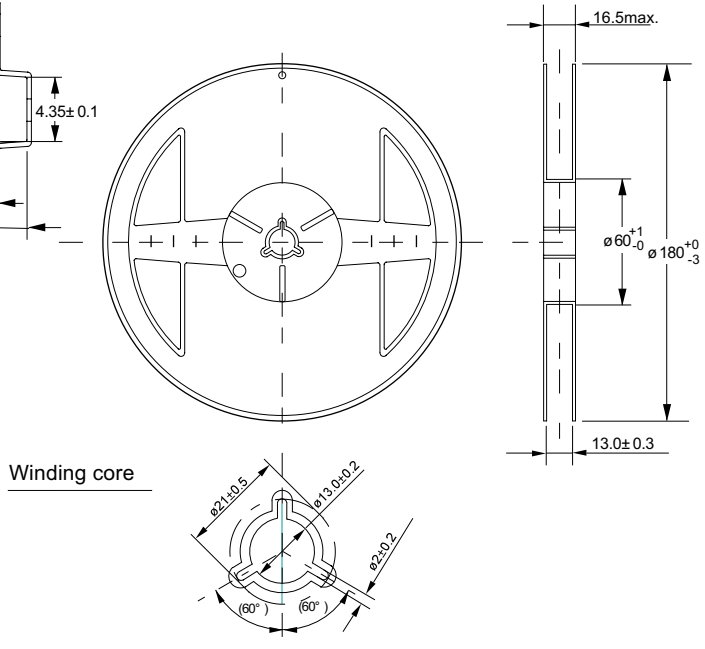



No. UP003-A-C-SD-1.0

## ●Reel Specifications

1 reel holds 1000 ICs.



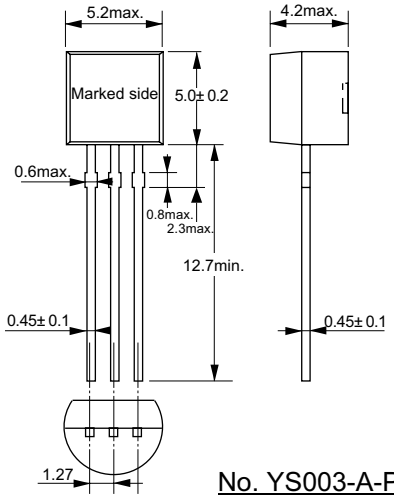

No. UP003-A-R-SD-1.0

# ■ TO-92

Unit:mm

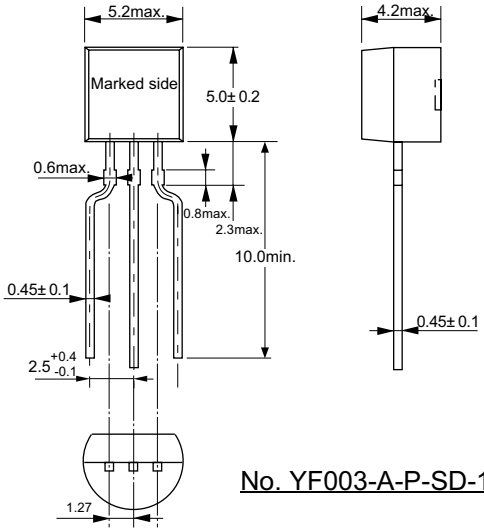
## ●Dimensions

(1) Bulk



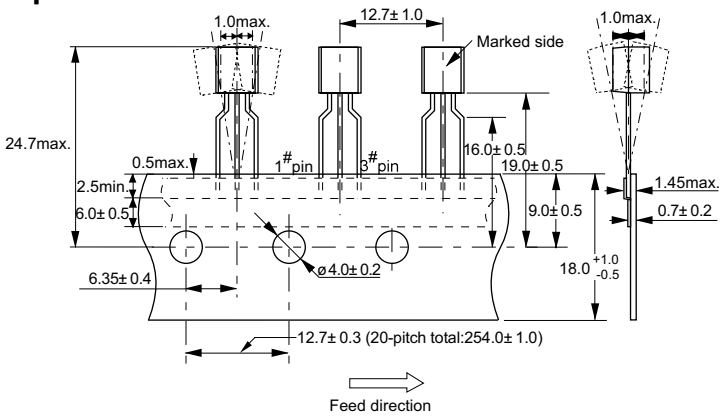

No. YS003-A-P-SD-1.0

(2) Leadforming for tape (reel/zigzag)

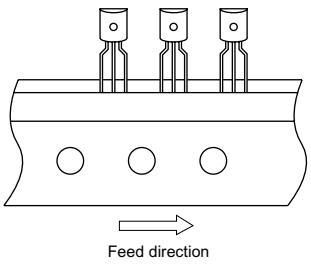



No. YF003-A-P-SD-1.0

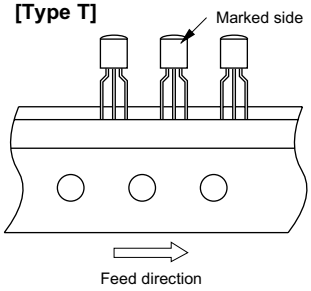
## ●Tape




[Type F]



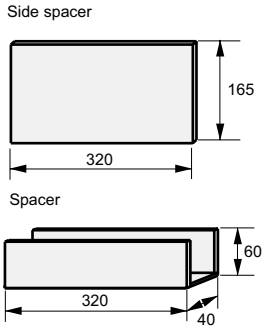

[Type T]

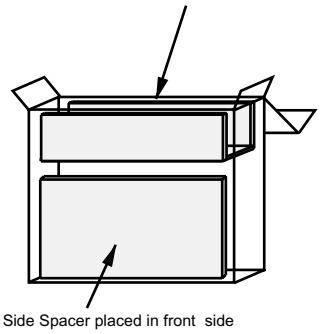



No. YF003-A-C-SD-1.0

## ●Zigzag

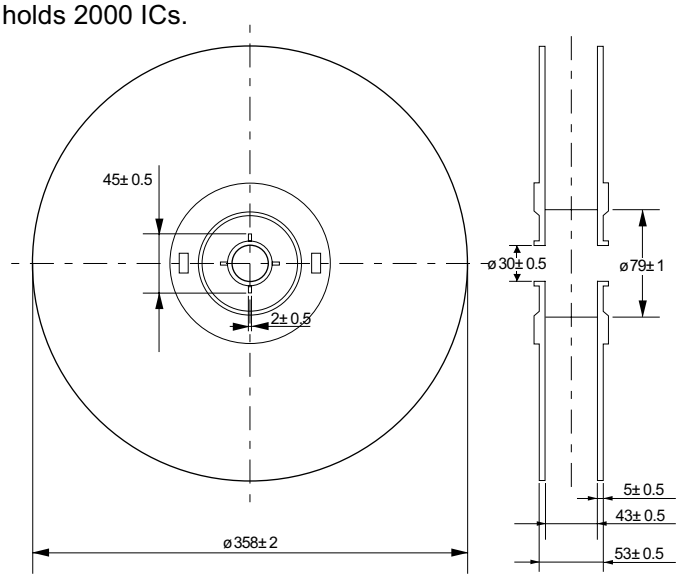
[Type Z]



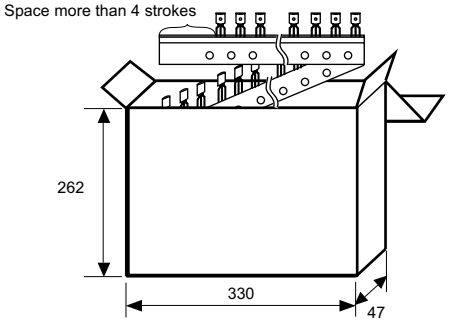

## ●Reel

1 reel holds 2000 ICs.

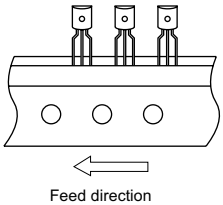



No. YF003-A-R-SD-1.0

Space more than 4 strokes




1 box holds 2500 ICs.

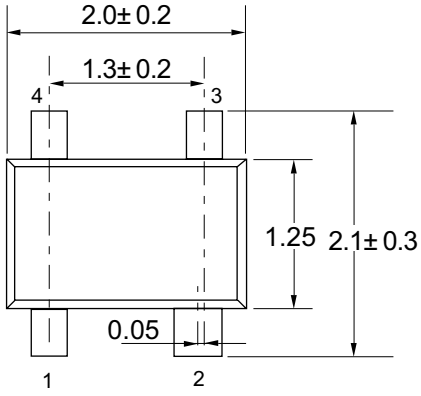


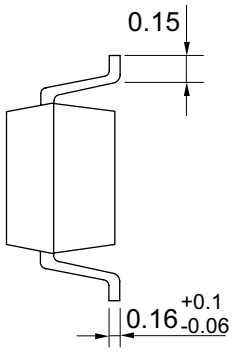

No. YF003-A-Z-SD-1.0

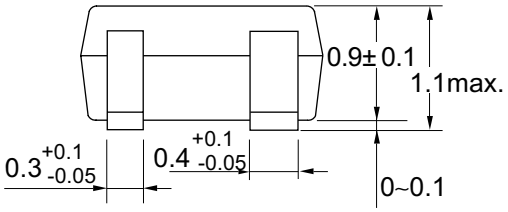
# ■ SC-82AB

Unit:mm

## ●Dimensions

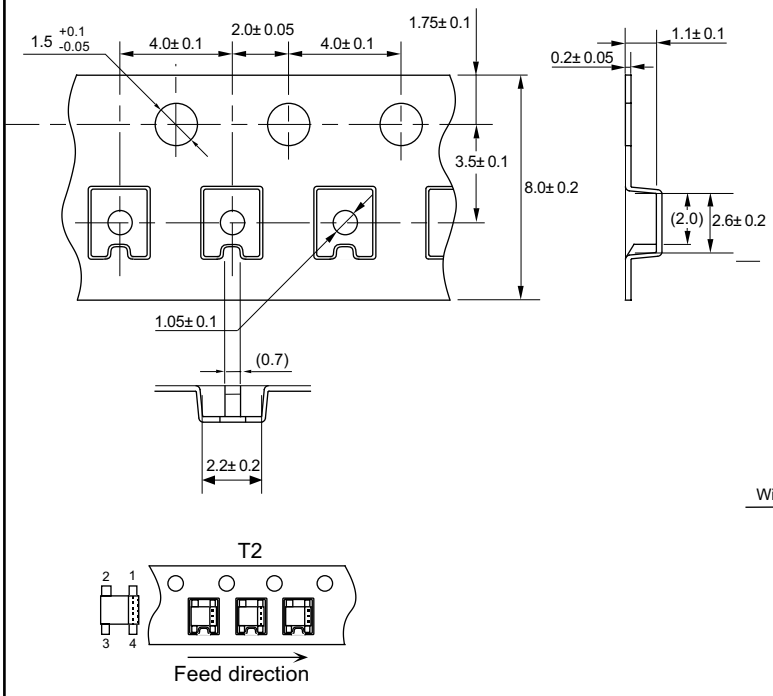



No. NP004-A-P-SD-1.0

## ●Taping Specifications





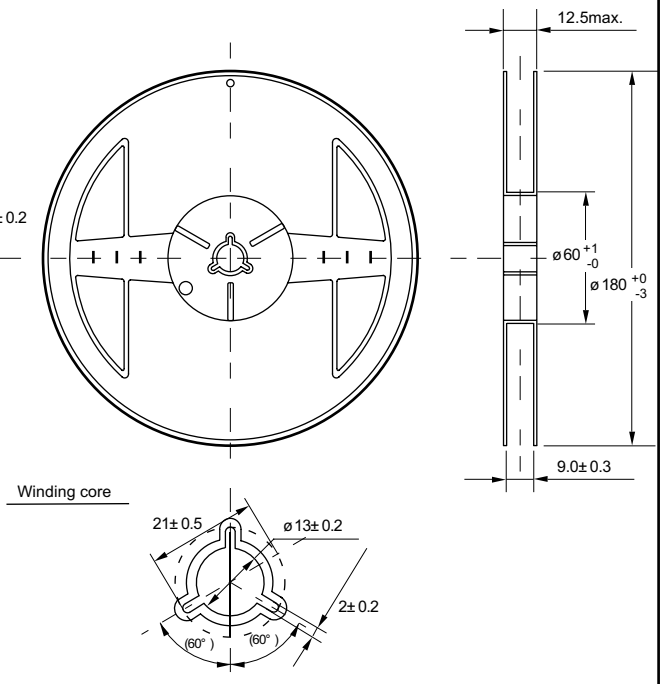





No. NP004-A-C-SD-1.0

## ●Reel Specifications

3000 pcs./ reel



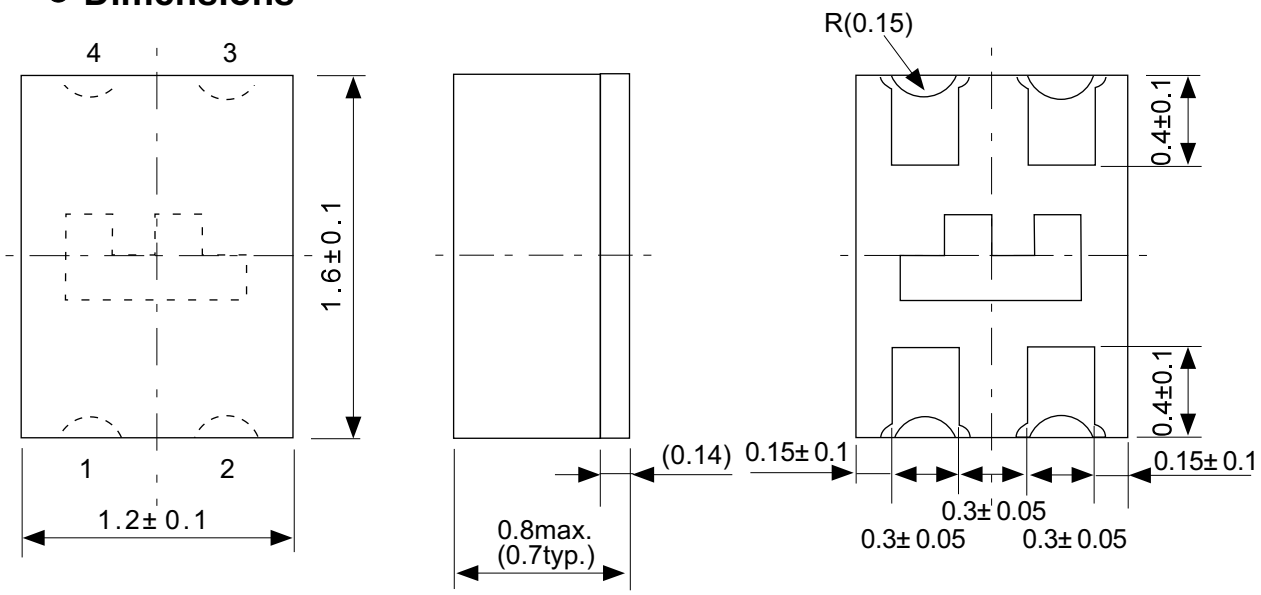

No. NP004-A-R-SD-1.0

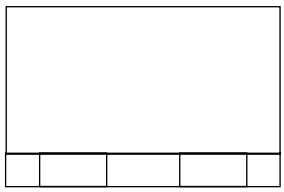
# ■ 4-Pin SNB(B) [SNB4B(1216)]

BB004-A 010801

Unit : mm

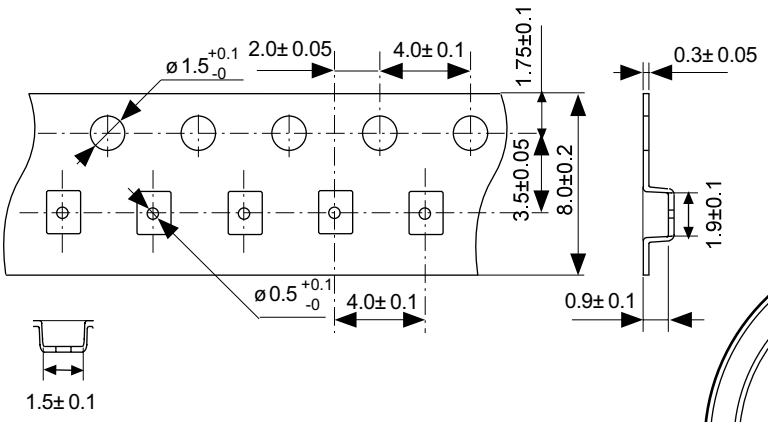
## ● Dimensions

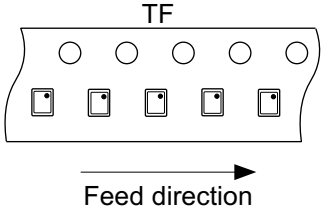


No. : BB004-A-P-SD-1.0

## ● Tape Specifications

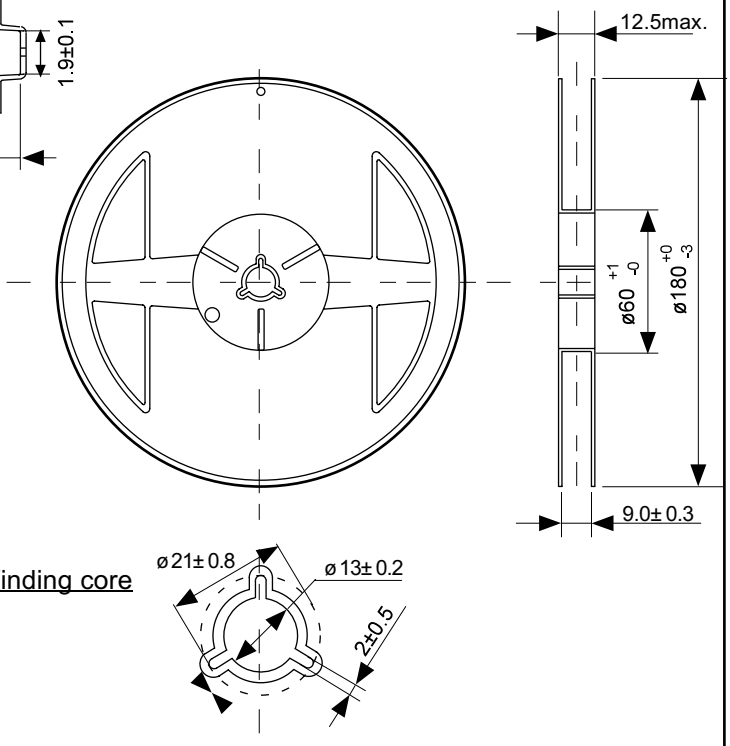



No. : BB004-A-C-SD-1.0

## ● Reel Specifications

5000 pcs./ reel



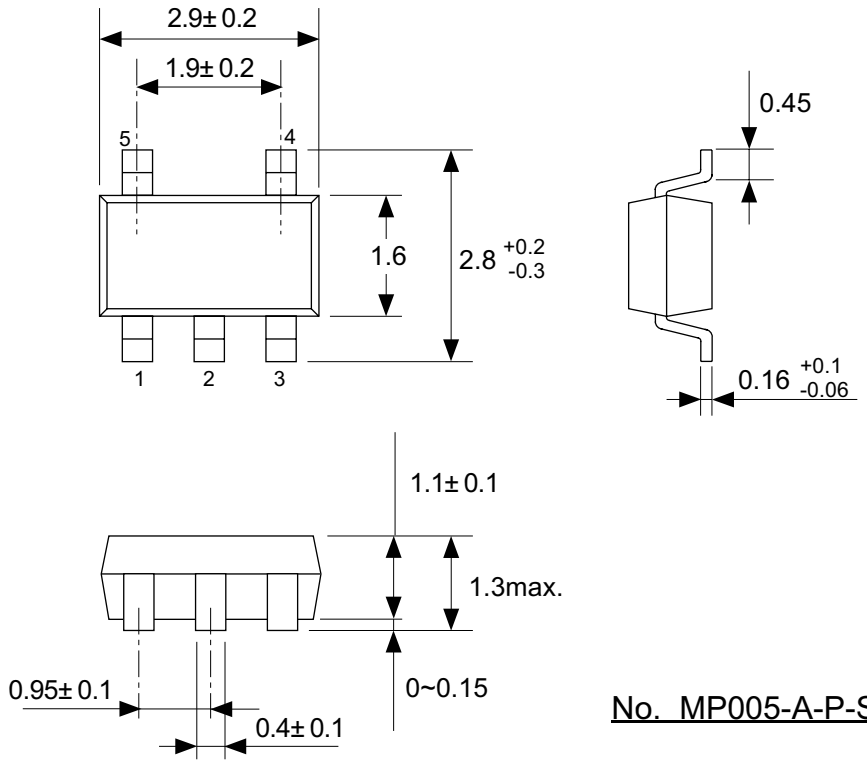

No. : BB004-A-R-SD-1.0

# ■ SOT-23-5

MP005-A 010801

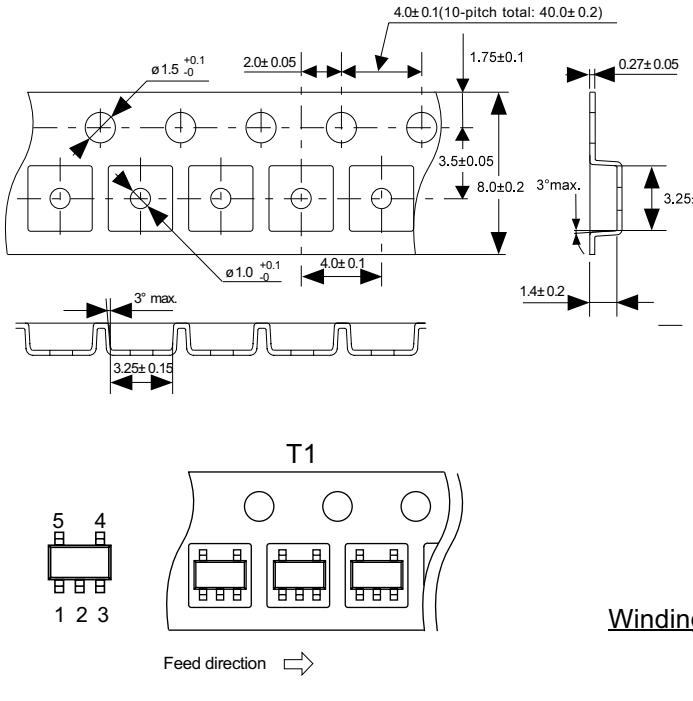
## ● Dimensions

Unit : mm




No. MP005-A-P-SD-1.1

## ● Tape Specifications



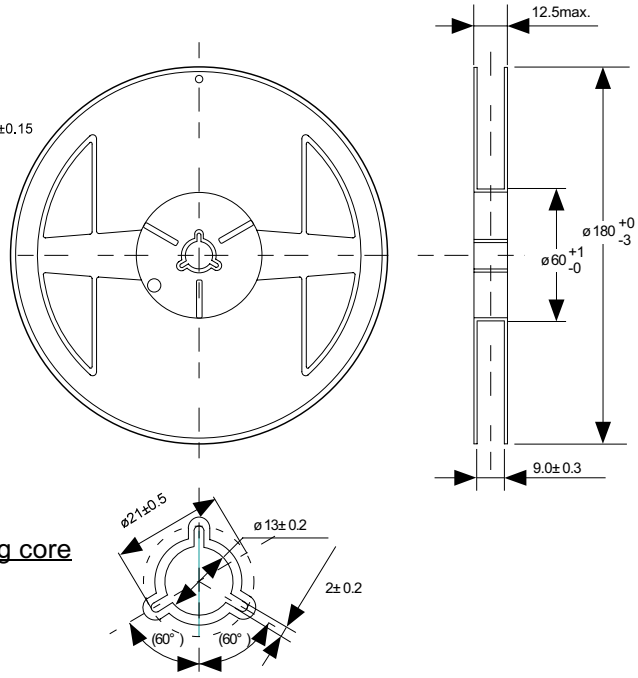




No. MP005-A-C-SD-1.0

## ● Reel Specifications

3000 pcs./reel




Winding core




No. MP005-A-R-SD-1. 0

- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.